Channel Recessed 4H-SiC MESFETs with F_t of 14.5GHz and F_{max} of 40GHz

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Abstract

Channel recessed 4H-SiC MESFETs have demonstrated excellent small signal characteristics and the effect of Si_3N_4 passivation on these devices has been studied in this work. A saturated current of 250-270 mA/mm and a maximum transconductance of 40-45 mS/mm were measured for these devices. The 3-terminal breakdown voltage V_{ds} ranges from 120 V to more than 150 V, depending on gate-drain spacing. 2 x 200 μm devices with 0.45 μm gate length show high F_t of 14.5 GHz and F_{max} of 40 GHz. After Si_3N_4 passivation, the output power and PAE were increased by 40% and 16%, respectively, for CW power measurement. Other measurements, such as, the change in surface potential and the dispersion of the drain current make it clear that the passivation of SiC MESFETs reduces the surface effects and enhances the RF power performance by suppressing the instability in DC characteristics.

I. Introduction

SiC MESFETs have emerged as promising high power microwave devices due to unique material properties, such as, high saturated electron velocity, high breakdown field, and high thermal conductivity. Wide bandgap semiconductor devices, such as, GaN HEMTs and SiC MESFETs have been developed for high power applications and have shown great potentials in comparison to GaAs and other commercially available devices. SiC MESFETs show better linearity than GaN HEMTs but operate at lower frequencies.

In this work, channel recessed 4H-SiC MESFETs were fabricated and they have demonstrated excellent small signal characteristics, such as, F_t of 14.5GHz and F_{max} of 40GHz. The device performance was compared to the case without channel recess that has also been fabricated on the same material. The improvement in small signal characteristics can be explained by a decrease in feedback capacitance and higher aspect ratio (L_g/a) that can enhance channel modulation and increase the ratio of G_m/G_o.

SiC MESFETs have been reported to have current instability and strong dispersion [1]. We present the effect of Si_3N_4 passivation on 4H-SiC MESFETs by measuring the instability of DC drain current, the dispersion of drain current with input power, the change in surface potential, etc. The Si_3N_4 passivation reduced surface trapping effect and enhanced the power performance. From our measurements, however, we found out that both the surface trapping and deep traps in the substrate can be responsible for the instability in SiC MESFETs.

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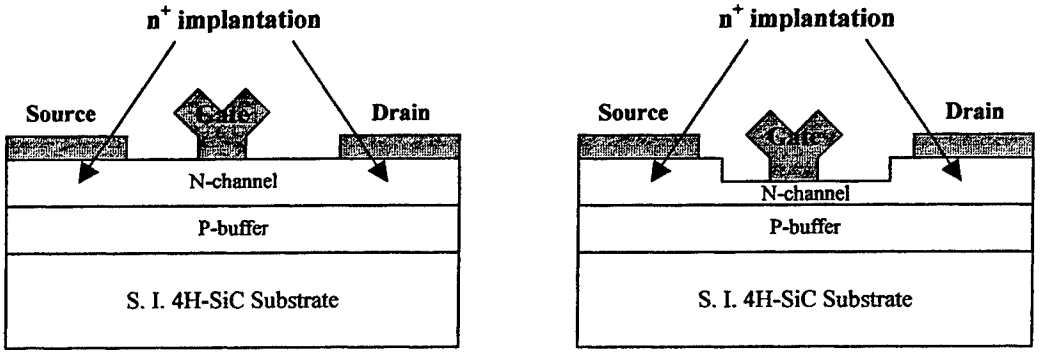
II. Device Fabrication

The material structure consisted of a semi-insulating 4H-SiC substrate, a 0.25 μm p-type buffer layer doped < 5 x 10^{15} cm^{-3}, and a 0.26 μm n-type channel layer doped N_d = 2 x 10^{17} cm^{-3}. The cross-sectional device designs are shown in Figure 1. Type I has no recess but type II has a channel recess region between source and drain. Source and drain regions were implanted with phosphorous. Ni deposition followed by annealing at 980°C resulted in a specific contact resistance of 1.5 x 10^{-6} Ω-cm^2. ECR etching with a $Cl_2/CH_4/Ar$ gas mixture was used to define the mesa and etch the channel region. The channel region between source and drain was etched 0.06 μm for the channel recessed device (Type II). The T-shaped gates were fabricated by multi-layer e-beam lithography process using a Cambridge EBMF10.5. The gates consisted of Ni/Pt/Au metal structure. A 1 μm thick Au layer was deposited as a pad and an ohmic overlay metal. PECVD Si_3N_4 passivation was done before the air-bridge step. The gate length was 0.4 μm and 0.45 μm for type I and type II, respectively. The source-to-gate spacing is fixed at 0.5 μm and the gate-to-drain spacings varied from 1.0 μm to 1.5 μm.



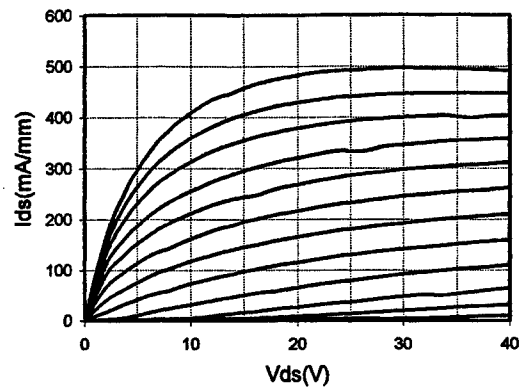
(a) Normal 4H-SiC MESFET without recess (Type I) (b) Channel recessed 4H-SiC MESFET (Type II)

Fig. 1. Cross-sectional design of 4H-SiC MESFETs utilizing phosphorus n^+ implantation

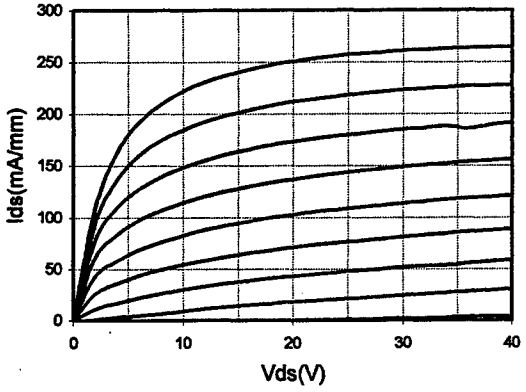
III. Results and Discussion

A. DC and Small Signal Characteristics

Figure 2 shows typical I-V characteristics of each type. Type I (Figure 2 (a)) showed higher current density but lower transconductance and lower breakdown voltage, as expected from no recess. A saturated current of 500 mA/mm and a maximum transconductance of 30 mS/mm were measured. According to the measurement, the pinch-off voltage, V_{gs}, is estimated to be less than -20V but the devices still showed a gate leakage of a few mA/mm for drain voltages greater than ~50V. The 3-terminal on-state breakdown voltage of 90V was observed. Type II, which had a channel recess, showed higher transconductance and breakdown voltage compared to type I. A saturated current of 250-270mA/mm and a maxium transconductance of 40-45mS/mm were measured. Negligible gate leakage (< nA/mm) was observed and a pinch-off voltage, V_{gs} ~ -8V was measured. The off-state 3-terminal breakdown voltage, V_{ds}, range from 120 V to more than 150 V at V_{gs} =-14V, depending on gate-drain spacing.



(a) Type I, Top trace is for V_{gs} = 0V, ΔV = -2V



(b) Type II, Top trace is for V_{gs} = 0V, ΔV= -1 V

Fig. 2. I-V characteristics of each type of devices

The unit current gain cut-off frequency (F_t) and maximun oscillation frequency (F_{max}) were extracted from s-parameters measured on-wafer using HP8510 network analyzer. This small signal measurement was done at V_{ds} = 20V and V_{gs} = -2V. Table I shows the values of F_t and F_{max} for each type of devices.

Table I. Small signal characteristics

	Cutt-off frequency (F_t)		Maximun oscillation frequency (F_{max})	
	Type I	Type II	Type I	Type II
2 x 100 μm	12.6 GHz	13.8 GHz	28 GHz	41 GHz
2 x 200 μm	N.A.	14.5 GHz	N.A.	40 GHz
2 x 300 μm	15.0 GHz	15.4 GHz	23 GHz	33 GHz
2 x 500 μm	18 GHz	16.0 GHz	17 GHz	18 GHz

We observed a trend in the small signal measurements with different unit gate width. The cut-off frequency increases with unit gate width due to higher gate capacitance. It is more significant on type I than type II. The highest F_t of 18GHz was obtained for 2 x 500 μm type I devices. As for shorter gate widths, higher F_t and F_{max} were obtained for type II devices. 2 x 200 μm type II devices demonstrated excellent F_t and F_{max} of 14.5 GHz and 40 GHz, respectively. Especially, F_{max} was significantly improved compared to type I (with F_{max} of 28 GHz). The improvement in small signal characteristics can be explained by considering the aspect ratio and feedback capacitance. The F_t and F_{max} of the device can be expressed by,

$$F_t = \frac{G_m}{2 \cdot \pi \cdot \left(C_{gs} + C_{gd}\right)} \quad (1)$$

$$F_{max} = \frac{F_t}{\sqrt{4\frac{Go}{Gm}\left(G_m \cdot R_i + \frac{Rs+Rg}{1/Gm+Rs}\right) + \frac{4}{5}\frac{Cgd}{Cgs}\left(1+\frac{2.5Cgd}{Cgs}\right)(1+G_m \cdot R_s)^2}} \quad (2)$$

The behavior of f_{max} is considerably more complicated since its value depends on the device resistances and feedback capacitance. The channel recess makes the depletion region between gate and drain extend more toward the edge of the drain, which can contribute to the decrease in the feedback capacitance. The channel recess also leads to higher aspect ratio (L_g/a), which improves channel modulation and increases the ratio of G_m/G_o. Therefore, the combination of high F_t, C_{gs}/C_{gd}, and G_m/G_o is a possible explanation for this dramatic improvement of F_{max}.

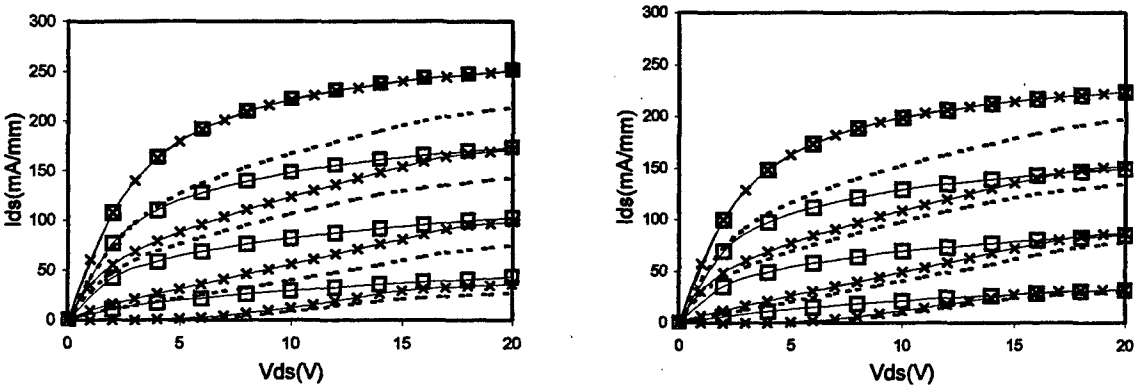
B. Current Instability and Passivation

SiC MESFETs have been reported to have current instability and strong dispersion. This phenomenon has been reported using a pulse IV measurement [1]. In this work, we illustrate this phenomenon by measuring IV characteristics using different bias sweeping method and surface potential using surface probing technique. These measurements were repeated under the same conditions after Si_3N_4 passivation. Figure 3 (a) shows the current instability of type II before passivation. Three different voltage sweeping were performed as followings.

(1) Case I (-□-) : From V_{gs} = 0V to V_{gs} = -10V with 100sec time interval between sweeps
From V_{ds} = 0V to V_{ds} = 20V (forward) at each gate bias
(2) Case II (-×-) : From V_{gs} = 0V to V_{gs} = -10V, No time interval
From V_{ds} = 0V to V_{ds} = 20V (forward) at each gate bias
(1) Case III (----) : From V_{gs} = -10V to V_{gs} = 0V, No time interval
From V_{ds} = 20V to V_{ds} = 0V (backward) at each gate bias

The gate voltage step was 1V, but only the cases of V_{gs} = 0V, -2V, -4V, and –6V were plotted for better understanding. The measurement for case I (-□-) was done with the time interval of 100sec between each gate voltage sweep while the others were done continuously. The time interval of 100sec is assumed to be enough to recover the state. Top two traces in Figure 3 are consistent with each other because of the same initial condition. We found discrepancy among different sweeping methods. For case II (-×-), current lag was observed and it was more significant at low drain voltages. The current recovers after reaching higher drain voltages. We speculate that trapping of electrons at the surface states and deep states in the substrate affect current lag phenomenon. With applied high drain bias, electrons can tunnel from the gate and move across the surface depletion region getting trapped at the surface states. In addition, electrons in the channel can pass through thin p-type buffer layer which is fully depleted under the high reverse bias condition and get trapped in the deep states present in the substrate [2]. Even after the drain voltage is disconnected (after the first sweep), the trapped electrons remain until they are slowly detrapped from the states. Consequently, unintentional depletion region is formed near the surface and lower channel region by the remaining electrons. Now, the channel area becomes thinner compared to the initial condition so that the channel current becomes lower. In the next sweep, this unintentional depletion region becomes covered by the extension of the gate-to-drain depletion and the p-n junction depletion as the applied drain voltage becomes higher again. Therefore, the current level recovers at higher drain bias region. Reasonably, this lag phenomenon is more serious for case III (----) because the higher field was applied between gate and drain at the previous sweep. Figure 3 (b) shows the same measurement result after passivation. Similar trends were observed but with noticeable improvement after passivation. This improvement was observed more significantly for the normal devices without channel recess.

To verify the effect of passivation on the surface, we also measured surface potential by using Kelvin probe technique. Detailed measurement procedures have been described elsewhere [3]. After stressing the device for 2 minutes with the drain voltage of 20V under the pinch-off condition, surface potential was measured versus time. Figure 4 shows the recovery of surface current versus time before and after passivation. Much faster recovery was observed after passivation, which proves that passivation reduces surface effect. In Figure 3 (b), however, current instability was not improved significantly. Surface treatment reduces instability, but not completely. We propose that current instability is caused not only by surface traps but also by deep traps in the substrate.



(a) Before passivation (b) After passivation

Fig. 3. Current instability before and after passivation (—□— : Forward drain voltage sweep with the time interval of 100sec for each gate bias, —×—: Forward drain voltage sweep from V_{gs} = 0 V toward –10 V without time interval, ——— : Backward drain voltage sweep from V_{gs} = –10 V toward 0 V without time interval)

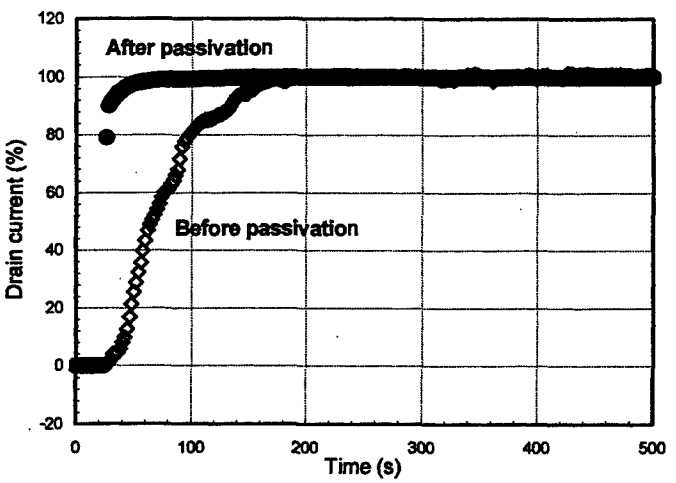


Fig. 4. The recovery of the surface current before and after passivation

Figure 5 shows the gate leakage current measured before and after passivation. Lower leakage current was observed after passivation for lower drain bias. However, it increases rapidly for higher drain bias in comparison to those before passivation. Passivation seems to prevent electrons from tunneling from the gate for lower drain bias but accelerate the tunneling mechanism for higher drain bias. The tunneling mechanism is closely related to temperature. Increased temperature on the surface around the gate in the high field region produces a decreased threshold voltage for the tunnel leakage so that thermally induced electrons can easily tunnel from the gate. [4] We speculate that it is more difficult to eliminate the increased surface temperature after passivation because the surface is blocked by passivation film. The thermal conductivity of Si_3N_4 is much less than that of SiC. Therefore, although passivation reduces the surface effect and suppress gate leakage for lower drain bias, more electrons can tunnel from the gate for higher drain bias by obtaining the thermal energy. These electrons flow toward the drain edge for higher drain bias, while most tunneling electrons can't arrive at the drain edge for lower drain bias. Moreover, passivation reduces the number of trapped electrons and therefore induces more electrons to reach the drain edge for higher drain bias. This can explain why the breakdown voltage reduces after passivation although the gate leakage current is lower for lower drain bias.

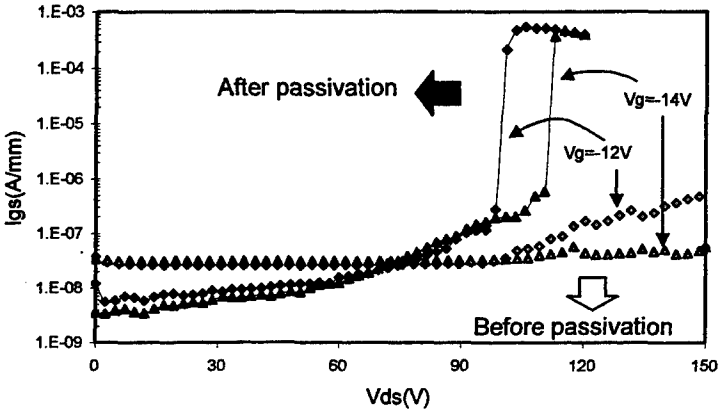
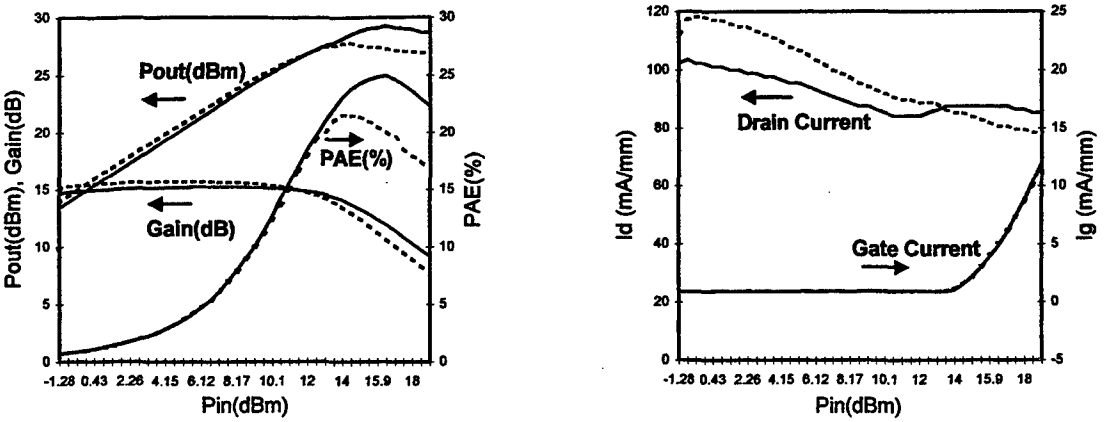


Fig. 5. Gate leakage current before and after passivation.

As shown previously, the channel recess resulted in lower saturation current but higher breakdown voltage. Figure 6 shows CW power measurements before and after passivation. CW power measurement was performed at 4 GHz with V_{ds}=30 V due to our measurement system limitation. The output power, gain, and PAE are plotted in Figure 6 (a) and the drain and gate current are plotted in Figure 6 (b). The unpassivated device showed output power density of 0.6 W/mm with the power gain of 15 dB and PAE of 20 %. Due to insufficient power sweeping at low drain bias, it showed relatively low output power. Compared to normal devices, the output power is a little lower but the power gain and PAE were improved. Especially, as expected from thinner channel region, the power gain was increased significantly, by a factor of 2. After passivation, the output power density of 0.85 W/mm was measured with PAE of 25% and a similar power gain for the channel recessed device. Although, the saturated current became lower after passivation, the output power and PAE were improved. This can be explained by investigating the drain current behavior versus input power in Figure 6 (b). While the drain current decreased continuously by 20-30% with input power before passivation, it decreased much less after passivation. This resulted in higher output power density and PAE compared to the unpassivated device for higher input power levels. The current drop reflects the instability in DC drain current shown in Figure 3.



(a) Output power, Gain, and PAE (b) Drain current dispersion versus input power

Fig. 6. CW power measurement before and after passivation at 4GHz (Vds=30V)
(Dashed lines : Before passivation, Solid lines : After passivation)

IV. Conclusion

Channel recessed 4H-SiC MESFETs have been fabricated and compared to normal devices without channel recess. The channel recess resulted in lower saturated current but higher breakdown voltage and excellent small signal characteristics. The cut-off frequency of 14.5 GHz and the maximum oscillation frequency of 40 GHz were measured on 2 x 200 μm devices with a gate length of 0.45 μm.

The current instability was observed by measuring I-V characteristics and surface potential. Si_3N_4 passivation improved current instability by reducing surface effects but cannot eliminate it completely. From these measurements, we propose that trapped electrons both on the surface and in the substrate modulate channel thickness by producing unintentional depletion region and therefore reducing the drain current.

Passivation reduces the gate leakage current for lower drain bias, but accelerates tunneling mechanism for higher drain bias. We speculate that the passivation film deposited on the surface makes it difficult to eliminate the increased surface temperature due to lower thermal conductivity. Therefore, thermally induced electrons can easily tunnel from the gate in the high field region and flow toward the drain to accelerate breakdown mechanism. Passivation also improves RF performance by suppressing the drain current dispersion with input power.

From our measurements, Si_3N_4 passivation on SiC MESFETs enhances device performance noticeably by the reduction of surface effects. However, it doesn't seem to be enough to completely eliminate the current instability. More study of deep traps in the substrate should be performed.

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